REMARKS

Applicant acknowledges the Examiner's request for clarification regarding the entry of an amendment to Claim 52 as requested in Applicant's September 28, 2000 response. The amendment is correctly entered.

Claims 41 and 43-52 are pending in the above referenced application. Claims 43, 44 and 47-49 are amended.

Rejection under 35 U.S.C.§112

Claims 43, 44 and 47-49 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention. Specifically, the Examiner identifies several locations where it is alleged that such claims lack proper antecedent basis. Applicant does not agree.

However, without admission, and only for the purpose of expediting the prosecution of the instant application, Applicant has amended Claims 43, 44 and 47-49 such that precise antecedent is maintained. Applicant therefore asserts, that the rejection of Claims 43, 44 and 47-49 is now moot. In addition, Applicant asserts that such amendments do not in any way alter the scope of such claims or subject such claims to any restriction as to the scope of equivalents upon which such claims read.

Rejections under 35 U.S.C. §102:

Kurimoto

Claims 41, 42, 45, 46 and 50 stand rejected under 35 U.S.C. §102(b), as being anticipated by Kurimoto (5,306,655). Applicant traverses.

The Examiner has maintained the instant rejection from the previous action, stating in the "Response to Arguments" at ¶ 6 of the Final Office Action, that "Kurimoto **also** recited a method (at column 18, lines 4-21) ... wherein an intervening oxide layer is not therefore formed" (emphasis added). Applicant respectfully asserts that such statement is misleading; lines 4-21 of column 18 are a portion of Kurimoto's Claim 1. Therefore in view of M.P.E.P. §608.01(g), which states that "[e]very feature specified in the claims must be illustrated," and since Kurimoto DOES NOT provide any illustration without an intervening oxide layer, Kurimoto's claim MUST refer to the embodiment the Examiner freely admits depicts an intervening oxide layer "figures 13a-13h, col. 13, lines 37-52 of Kurimoto show an intervening oxide layer," (¶ 6 of the Final Office Action).

Therefore Claim 41, which recites, in pertinent part, "forming sidewall spacers comprising nitride over the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer" is NOT anticipated by Kurimoto. Applicant respectfully requests the instant rejection of Claim 41 be withdrawn.

Claims 45 and 50 contain pertinent language similar to that of Claim 41. Specifically, Claims 45 and 50 recite, respectively, among other things:

> (45) forming sidewall spacers laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material
>
> (50) forming non-oxide material over the gate structure and the dielectric layer;
> anisotropically etching the non-oxide material to form spacers over the sidewalls, the spacers laterally adjacent the gate structure and joining with the gate dielectric layer there at.

Thus, as stated above with regard to Claim 41, Kurimoto CANNOT anticipate Claims 45 and 50. Claim 46 depends from Claim 45, therefore, for at least the same reason as for Claim 45, Kurimoto cannot anticipate Claim 46. Hence Applicant requests that the instant rejection of Claims 45, 46 and 50 be withdrawn. It then follows that Claims 41, 45, 46 and 50 are in condition for immediate allowance, which action is earnestly sought.

Verhaar, with Hiroki as evidence or in the alternative under §103(a)

Claims 41, 45, 46 and 50 stand rejected under 35 U.S.C. §102 (b) as being anticipated by Verhaar (5,015,598), with Hiroki et al. (5,512,771, hereinafter "Hiroki") as evidence, or in the alternative under 35 U.S.C. §103(a). Applicant traverses.

Applicant's Claims 41, 45 and 50 each recite, respectively, among other things:

> (41) exposing the substrate to oxidizing conditions ... wherein a portion of the gate electrode, laterally adjacent the

sidewall spacers and at the interface with the gate dielectric layer, is oxidized

(45) conducting an oxidizing step ... wherein the oxidation resistant sidewall spacers provide that only a portion of the gate electrode, adjacent the oxidation resistant sidewall spacers and at the interface with the first layer, is oxidized

(50) exposing the substrate to oxidizing conditions effective to oxidize only that portion of the gate structure adjacent the spacers and the dielectric layer

Therefore, in each of Applicant's rejected independent claims, the referred to oxidation results in a portion of the gate electrode being oxidized.

In contrast, Verhaar, does not oxidize a portion of the gate electrode, but rather provides oxidation conditions effective to "regenerate the parts of insulating gate layer 11." These parts being identified as the ends of layer 11 that have become degraded and/or polluted by the etching of poly layer 12 and the forming of source and drain regions 22 and 23 by ion implantation 21 (col. 4, lines 19-32). The Examiner alleges, however, that the oxidation conditions of Verhaar inherently cause the oxidation of portions of the gate electrode to create a "smiling gate." The Examiner is mistaken.

The Examiner's inherency argument seems based on, in significant part, the specification at page 7, lines 14-19 wherein Applicant essentially states that the gate electrode is oxidized in a time period for growing an oxide layer over the semiconductor substrate to a thickness of about 80 Å, and Verhaar's statement that a silicon oxide layer 24 having a thickness of 100 to 150 Å is formed. The Examiner's conclusion seems to be that since the thickness of Verhaar's oxide is greater than that

described by the Applicant, the gate electrode of Verhaar is **inherently** oxidized.

However, the Examiner fails to consider that Verhaar teaches forming source and drain regions 22 and 23, heavily doped with phosphorus, prior to providing oxidation conditions and that the amount of oxide growth in such heavily doped regions is significantly enhanced. Such enhanced growth is discussed Wolf et al. in *Silicon Processing for the VLSI Era*, Vol. 1, Second Edition, (Lattice Press, 2000) at pages 278-280, a copy of such pages is provided for the Examiner's reference. Referring to Fig. 8-10, Wolf et al. show that a 30 minute oxidation of such phosphorus doped silicon at about 900°C will result in oxide growth of 1000 Å or more. Therefore, where Verhaar recites that such oxide layer 24 is formed having a thickness of 10 to 15 nm, it is necessary that the time taught by Verhaar is much too short for there to be <u>any</u> oxidation of the gate electrode. Since Wolf et al. is recognized as an authority in the field of semiconductor processing, Applicant respectfully asserts that the burden imposed by *In re King*, referenced by the Examiner in the Final Office Action, is met and the instant rejection is shown to be in error. Claim 46 depends from Claim 45, therefore for at least the same reason as for Claim 45, the rejection of such dependent claim is also in error. It follows then that the rejection under §102(b) of Claims 41, 45, 46 and 50 must be withdrawn.

With regard to the rejection under §103(a), in the alternative, the Examiner states that Hiroki teaches that "oxide layer 6' formed under silicon nitride spacer 7 allows oxidizing substance to transmit

therethrough to oxide a portion of the gate electrode" (¶ 3, page 4 of the Final Office Action). However, Applicant respectfully points out that the structure of Hiroki provides layer 6' as an intervening oxide layer between silicon nitride layer 7 and the sidewalls of the gate electrode. The structure of Hiroki is analogous to that of Kurimoto shown in Fig. 13d. Hence for at least the same reasons as put forth in the discussion of Kurimoto in both this response and in Applicant's previous response, incorporated herein, Hiroki CANNOT provide either the evidence the Examiner attributes to it or can it make Applicant's invention as recited in Claims 41, 45, 46 and 50 obvious.

While the Examiner makes no statement that a combination of Verhaar and Hiroki is envisioned as making the instant claims unpatentable, Applicant respectfully asserts that such a combination, if offered in a subsequent action, is inappropriate. Verhaar teaches that only the regeneration of the polluted silicon oxide under the nitride spacer is desired. The structure of Hiroki, having the intervening oxide layer 6', would prevent such limited oxide growth. Hence making Verhaar unsuitable for its intended purpose. Such a result is well established as proof that such a combination is NOT obvious (M.P.E.P. §2143.01).

Rejections under 35 U.S.C. §103:

Kurimoto or Verhaar/Hiroki in view of Pintchovski et al.

Claims 43 and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over either Kurimoto or Verhaar/Hiroki in view of Pintchovski et al. (5,126,283, hereinafter "Pintchovski"). Applicant Traverses.

Claims 43 and 47 depend from Claims 41 and 45, respectively. In the remarks presented above, and reasserted for the instant rejection, for each of Kurimoto, Verhaar and Hiroki, as well as for the combination of Verhaar and Hiroki, Applicant has shown that the Examiner's argument for rejection based on such art is incorrect. In summary, it has been shown that Kurimoto does not teach an alternative embodiment that is absent an intervening oxide layer; that Verhaar does not teach oxidation conditions sufficient to oxidize a portion of the gate electrode; that Hiroki depicts a structure having an intervening oxide layer in a manner analogous to that of Kurimoto and that a combination of Verhaar and Hiroki would render Verhaar unsatisfactory for its intended purpose. Since Pintchovski is not offered by the Examiner to remedy any of these defects, and since it does not in fact provide any such remedies, Applicant respectfully asserts that any rejection under §103 based on a combination of Kurimoto with Pintchovski or Verhaar/Hiroki with Pintchovski is necessarily incorrect as no such combination teaches or even suggests all aspects of the invention recited in either Claim 43 or 47. It follows then that the instant rejection must be withdrawn. Action to this effect is requested.

Kurimoto or Verhaar/Hiroki, in view of Pintchovski and further in view of Brigham et al. and Kumagai et al.

Claims 44, 48, 49, 51 and 52 stand rejected under 35 U.S.C. §103(a) as being unpatentable over either Kurimoto or Verhaar/Hiroki, in view of Pintchovski as applied to Claims 41, 43, 45-47 and 50 above, and further in view of Brigham et al. (5,714,413, hereinafter "Brigham") and Kumagai et al. (5,430,313, hereinafter "Kumagai"). Applicant Traverses.

As stated in Applicant's response to the preceding rejection, Applicant has shown that the Examiner's argument for rejection based on Kurimoto, Verhaar, Hiroki and Verhaar combined with Hiroki is incorrect. Such response is reasserted for the instant rejection. As neither Brigham or Kumagai are offered to correct the deficiencies of the bas art employed for the instant rejection, and as neither in fact provides such teachings or even suggests such teachings, the instant rejection is incorrect and must be withdrawn. Action to this effect is requested.

In summary, Applicant having remarked to each of the rejections presented by the Examiner in the above-referenced Final Office Action, respectfully request reconsideration of the instant application in view of these remarks. In each case Applicant has shown the rejection to be incorrect. Therefore, Applicant respectfully asserts that the all the claims of the application presented in this RCE filing are in condition for allowance. Action to that effect is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic

interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: April 16, 2001 By: Bernard Berman

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/059,644
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Inventor ..... Pai-Hung Pan
Assignee ..... Micron Technology, Inc.
Group Art Unit 2822
Examiner ..... M. Trinh
Attorney's Docket No. MI22-898
Title: Semiconductor Processing Method Of Forming A Conductive Gate And Line

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 19, 2000 OFFICE ACTION

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

43. The method of claim 41, wherein the gate electrode comprises a first conductive layer a portion of which defines the interface, an overlying metal layer, and an electrically conductive reaction barrier layer interposed between the first layer and the overlying layer.

44. The method of claim 41, wherein the forming of the sidewall spacers includes:

depositing a first material over the gate electrode;

depositing a second material over the first material;

anisotropically etching the first and second materials to a degree sufficient to leave the spacers over the gate's sidewalls, the spacers being defined by both the first and second material.

47. The method of claim 45, wherein the gate ~~stack~~ structure comprises a polysilicon layer, an overlying metal layer, and an electrically conductive reaction barrier layer intermediate the polysilicon layer and the overlying metal layer.

48. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate ~~stack~~ structure;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the sidewall spacers over the gate ~~stack's~~ structure's sidewalls.

49. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate ~~stack~~ structure;

anisotropically etching the first material to a degree sufficient to leave first sidewall spacers over the gate ~~stack~~ structure;

depositing a second material over the first sidewall spacers; and

anisotropically etching the second material to a degree sufficient to leave second sidewall spacers over the first sidewall spacers.